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EXAMINER	
NGUYEN, MIKE	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/494,787	MOUNT, JOHN A.	
	Examiner	Art Unit	
	Mike Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notices & Remarks

1. Applicant's amendment 03/04/2005 in response to Examiner's Office Action has been reviewed. The following rejections now apply.

2. Claims 1-20 are pending for the examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Liu (U.S. Pat. No. 5,768,617).

As to claim 1, Liu teaches in a storage system (fig. 2) having a bus (computer data bus 215) operatively coupled to a first controller chip (storage controller integrated circuit 230) and a first channel chip (computer bus interface circuit 234), the channel chip having several registers (fig. 3), the storage system also having a storage medium (disk 240) operatively coupled to the bus through a storage medium interface (drive electronic 223), a method for retrieving data record on a storage medium comprising the step of:

(a) retrieving a first portion of the record data via the bus (col. 8 lines 28-34, 61-64);

(b) updating some of the registers via the bus (col. 8 lines 34-49, 64-67); and

(c) retrieving a second portion of the record data via the bus (col. 8 lines 43-49 and col. 9 lines 3-12).

As to claim 16, Liu teaches a method comprising steps of:

(a) providing data via a bus (computer data bus 215 of fig. 2 and col. 8 lines 28-34, 61-64);

(b) updating at least one register or parameter via the bus (fig. 3 and col. 8 lines 34-49, 64-67); and

(c) providing data via the bus responsive to the updating (col. 8 lines 43-49 and col. 9 lines 3-12).

As to claims 17-18, Liu teaches the bus is serial and parallel (fig. 3).

As to claim 19, Liu teaches the method of claim 16 wherein the steps are controlled by a processor (auto-read sequencer 250 and auto-write sequencer 260 of fig. 2).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu in view of Cloke (U.S. Pat. No. 6,411,452 B1).

As to claims 2-5, Liu fails to explicitly teach a read head, plurality of operating parameters, at least one read channel parameter value, and at one mode-indicative value. Cloke;

however, teaches the interface includes the read head (fig. 1A element 19 col. 8 line 19) further comprising a step (d) of repositioning the storage medium interface with respect to the storage medium (col. 8 lines 20-32 wherein the read head is used to position the interface) between retrieving step (a) and (c) and has a plurality of operating parameters that are modified in updating step (b) (col. col. 22 lines 5-7), and the registers contain at least one read channel parameter value selected from the group consisting of: a precompensation value, a filter coefficient value, and a phase offset value; and at least one mode-indicative value (see col. 25 lines 2-12). It would have been obvious to a person of ordinary skill in the art to have the read head, plurality of operating parameters, at least one read channel parameter value, and at least one mode-indicative value in order to control read and write operations performed by the read channel.

7. Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu in view of Bowes et al. (U.S. Pat. No. 5,828,856).

As to claim 15, Liu teaches a disc drive (fig. 2) comprising:

at least one disc (disk 240 of fig. 2);

an interface configured to read data from the at least one disc (drive electronic 223 of fig. 2 and col. 7 lines 8-11);

a memory containing several values indexed by zone identifiers (RAM 222 of fig. 2 and col. 13 lines 21-28);

a first controller chip (storage controller IC 230 of fig. 2) containing a microprocessor (microprocessor 221) and buffer controller 233, the controller operatively coupled to the memory (fig. 2);

a first channel chip having several register (computer bus interface circuit 234 of figs 2 and 3); and

a bus operatively coupled between the interface and the chips (computer data bus 215 of fig. 2), the bus controllable by the controller to read from the memory and to update several of the registers in response to a Zone transition event (col. 8 line 28 to col. 9 line 12).

Although Liu teaches substantial features (discussed above), he fails to explicitly teach the controller is a direct memory access (DMA) controller. Bowes; however, teaches the DMA controller (fig. 2A element 222). It would have been obvious to a person of ordinary skill in skill of the art to have the DMA controller in order to alleviate the CPU of the task (col. 1 lines 30-32).

As to claim 20, Liu teaches a controller (buffer controller 233 of fig. 2) but he fails to explicitly teach a direct memory access apparatus. Bowes; however, teaches the direct memory access apparatus (fig. 2A element 222). It would have been obvious to a person of ordinary skill in skill of the art to have the direct memory access apparatus in order to alleviate the CPU of the task (col. 1 lines 30-32).

8. Claims 6-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu, and Cloke in view of Bowes et al.

As to claim 6, Liu teaches in a storage system (fig. 2) having a disc (disk 240 of fig. 2), an interface (drive electronic 223) configured to read data, a value table indexed by zone identifiers (RAM 22 of fig. 222 and col. 13 lines 21-28), a controller (buffer control 233 of fig. 2), a microprocessor (microprocessor 221 of fig. 2) coupled to the controller, and several read

channel registers each containing value (computer bus interface circuit 234 of figs 2 and 3), a method comprising steps of:

(a) retrieving via the controller several values indexed by zone identifier Zb (col. 7 line 37 to col. 8 line 33);

(b) updating at least some of the read channel register values from the retrieved values (col. 8 lines 34-39, 64-67);

(c) reconfiguring the interface to read data in zone Zb (col. 8 lines 44-46 and col. 9 lines 3-6); and

(d) reading the target segment (col. 8 lines 44-46 and col. 9 lines 3-6);

Cloke teaches at least two zones having zone identifiers Za and Zb (see fig. 2B elements 62, 64, Di, Si col. 25-29);

Although Liu and Cloke teach substantial features (discussed above), they fail to explicitly teach a direct memory access (DMA) controller. Bowes; however, teaches the DMA controller (fig. 2A element 222). It would have been obvious to a person of ordinary skill in skill of the art to have the DMA controller in order to alleviate the CPU of the task (col. 1 lines 30-32).

As to claim 7, Cloke teaches the target segment has a predetermined starting track number, further comprising step of deriving zone identifier Zb from the predetermined starting track number before retrieving step (a) (col. 16 lines 33-60).

As to claim 8, Cloke the interface includes at least one head (fig. 1A element 19 col. 8 line 19), in which positioning step (c) includes a step (c1) moving the at least one head radially across the disc, the moving step (c1) beginning before retrieving step (a) is complete (col. 8 lines 20-32 wherein the head is used to position the interface prior initiating read/write operations in the new data zone band).

As to claim 9, Cloke teaches moving step (c1) before retrieving step (a) (col. 8 lines 20-32 wherein the head is used to position the interface prior initiating read/write operations in the new data zone band).

As to claim 10, Cloke teaches zone Zb has a corresponding data rate Rb that is not in common with zone Za (col. 14 line 67 to col. 15 line 1 wherein the channel frequency will increase in an outward radial direction so that data rate will be different in each zone band), in which position step (c) includes a step of (c2) sampling a signal from the interface at an initial frequency that is an integer multiple of data rate Rb (col. 14 line 60 to col. 15 line 14).

As to claim 11, Cloke teaches further comprising prior steps of:

(e) reconfiguring the interface to read data in zone Zb (col. 10 lines 14-31 and col. 14 lines 55-59 wherein the channel 26 configures the interface 22 to read/write data in zone bands);

(f) receiving a signal from the interface (col. 15 lines 43-48);

(g) deriving several values indicative of the interface's performance in zone Zb from the received signal (col. 22 lines 42-60); and

(h) storing of the derived values in the value table each at a position associated with zone Zb (col. 22 lines 46-50).

As to claim 12, Liu teaches the storage system includes an integrate circuit (integrated circuit 230 of fig. 2) comprising the microprocessor, and in which the retrieving step (a) comprises issuing at least one but fewer than 10 commands from the microprocessor to the controller (col. 7 lines 37-52).

As to claim 13, Cloke teaches the method of claim 12 further comprising steps of:

(j) sensing position data from a servo sector via the interface (col. 32 lines 54-65); and

(k) deriving a servo control signal from the sensed position data with the microprocessor during step (b) (col. 41 lines 30-37).

As to claim 14, Liu teaches a printed circuit board assembly (element 220 of fig. 2) including a memory containing the value table (RAM 22 of fig. 2 and col. 13 lines 21-28), the storage system comprising:

a master integrated circuit (IC) (storage controller integrated circuit 230 of fig. 2) containing the microprocessor (microprocessor 221) and the controller (buffer control 233), the controller being operatively coupled to the memory (fig. 2);

a slave IC containing the several read channel registers (computer bus interface circuit 234 of figs 2 and 3); and

a bus coupled between the master IC and the slave IC (computer data bus 215 of fig. 2), the bus controlled by the controller to perform updating (b) (col. 8 line 28 to col. 9 line 12).

Response to Arguments

9. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is 571 272-4153. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 571 272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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05/09/2005